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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,282	03/30/2004	Yasutaka Nakashiba	8008-1052	2273

466 7590 04/21/2005

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/812,282	NAKASHIBA, YASUTAKA
	Examiner	Art Unit
	Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, as disclosed in figures 1A-1C and their description on pages 1-7 of the instant application, in view of Von Basse et al. (UK Patent Application 2030768A). With regard to Claim 1, Applicant's admitted prior art discloses a semiconductor integrated circuit device comprising:

a substrate (Psub), formed of P-type silicon (page 1, lines 24-25 of the instant application);

MOS transistors (page 1, lines 18-19 of the instant application), including an N-channel MOS transistor (1) and a P-channel MOS transistor (2), disposed (see figures 1A and 1B of the instant application) in said substrate (Psub) and which include gate insulating films (4) for each MOS transistor; and

a MOS-type varactor element (23) disposed (figure 1C of the instant application) in said substrate (Psub) and which includes a gate insulating film (4), similar to that of N-channel MOS transistor (1) and a P-channel MOS transistor (2).

Applicant's admitted prior art fails to disclose the claimed gate insulating film of the MOS type varactor element having a thickness thinner than the thinnest gate insulating film among said gate insulating films of the MOS transistors. However, Von Besse discloses (Specification, page 1, lines 121-128) a semiconductor device, which includes a MOS transistor (AT) and a capacitor (CS) arranged beside one another on a P-doped silicon semiconductor substrate (SU), wherein the capacitor (CS) is a depletion-type varactor (Specification, page 2, lines 33-36). The gate oxide film (GOS) of the varactor and the gate oxide film (IS) of the transistor are formed from the same material and at the same time, as can be seen from the cross-hatching on figure 2. The depletion-type varactor is formed, when in deletion mode, by reducing the thickness (Specification, page 2, lines 36-40) of the gate oxide layer (GOS) of the varactor in comparison to the gate insulating film (IS) of the MOS selection transistor (AT), as clearly shown in figure 2 of Von Besse. Thus, the reference clearly suggest forming a gate oxide film of the varactor having a thickness thinner than that of the transistor.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed gate insulating film of the MOS type varactor element having a thickness thinner than the thinnest gate insulating film among said gate insulating films of the MOS transistors, as suggested by Von Besse, in order to achieve a high capacitance for the varactor structure (Specification, page 2, lines 45-47).

With regard to Claim 2, a further difference between the claimed invention and Applicant's admitted prior art is, the claimed maximum gate voltage applied to the MOS type varactor being lower than a maximum gate voltage applied to the MOS transistors. However, Von Besse discloses (Specification, page 2, lines 52-55) a depletion-type varactor (Specification, page 2, lines 33-36) operating at a ground operating voltage of 0, which is obviously lower than a gate voltage needed to drive the MOS transistor (AT), since as commonly known, the MOS transistor needs a gate voltage for proper operation. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed maximum voltage applied to the MOS type varactor being lower than a maximum gate voltage applied to the MOS transistors, as suggested by Von Besse, in order to reduce fluctuations and increase the security of the stored information in the capacitor (page 2, lines 55-58).

With regard to Claims 3 and 4, Applicant's admitted prior art discloses a semiconductor substrate (page 1, lines 18-23 of the instant application).

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
4/15/05

GEORGE ECKERT
PRIMARY EXAMINER